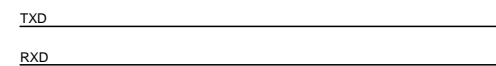
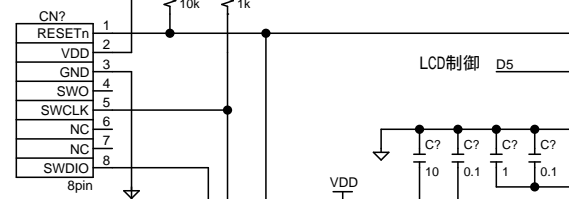


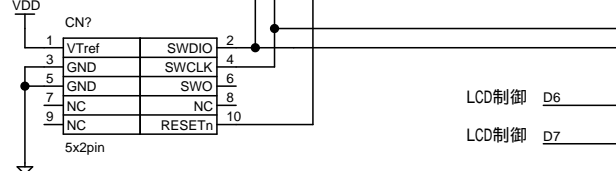
CAN通信0



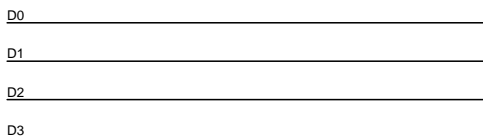
PICKIT4
コネクタ



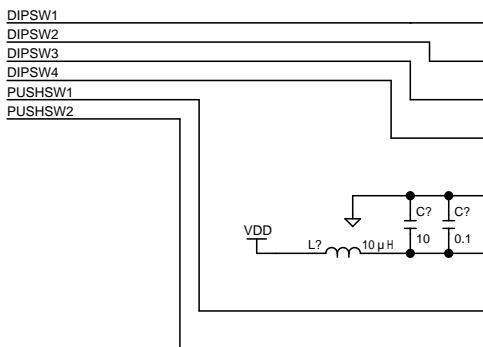
Atmel-ICE
コネクタ



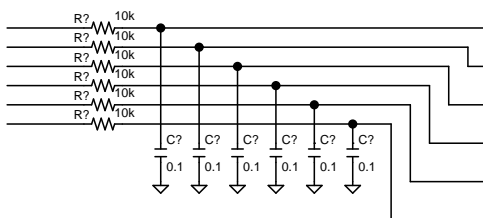
LCD制御



SW入力



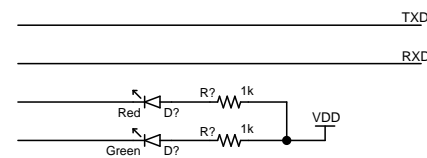
アナログ入力



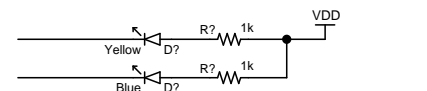
U7 ATSUMC21J

VDDIN系ポート (C20) VDDIO系ポート (C21)		VDDIO系ポート	
49	PB22/E.6/U3.0/G.0/(S5.2/CAN0.TX)	17	PA08/NMI/A.8/S0+0/S2+0/T0.0/T1.2/(A.10)
50	PB23/E.7/U3.1/G.1/(S5.3/CAN0.RX)	18	PA09/E.9/A.9/S0+1/S2+1/T0.1/T1.3/(A.11)
		19	PA10*/E.10/A.10/S0.2/S2.2/T0.0/T0.2/G.4
		20	PA11*/E.11/A.11/S0.3/S2.3/T1.1/T0.3/G.5
51	PA27/E.15/G.0	21	VDDIO
52	RESETn	22	GND
53	PA28/E.8/G.0		
54	GND	23	PB10*/E.10/U1.0/T0.4/G.4/(S4.2/CAN1.TX)
		24	PB11*/E.11/U1.1/T0.5/G.5/(S4.3/CAN1.RX)
55	VDDCORE	25	PB12/E.12/U0.0/T0.6/G.6/(S4+0)
56	VDDIN	26	PB13/E.13/U0.1/T0.7/G.7/(S4+1)
57	PA30/SWCLK	27	PB14/E.14/U1.0/G.0/(S4.2/CAN1.TX)
58	PA31/SWDIO	28	PB15/E.15/U1.1/G.1/(S4.3/CAN1.RX)
59	PB30/E.14/T0.0/T1.2/C.2/(S5+0)		
60	PB31/E.15/T0.1/T1.3/C.3/(S5+1)	29	PA12/E.12/S2+0/T2.0/T0.6/C.0/(S4+0)
		30	PA13/E.13/S2+1/T2.1/T0.7/C.1/(S4+1)
61	PB00/E.0/U3.0/(A.0/S5.2)	31	PA14/XIN/E.14/S2.2/U4.0/T0.4/G.0/(S4.2)
62	PB01/E.1/U3.1/(A.1/S5.3)	32	PA15/XOUT/E.15/S2.3/U4.1/T0.5/G.1/(S4.3)
63	PB02/E.2/U2.0/(A.2/S5.0)		
64	PB03/E.3/U2.1/(A.3/S5.1)	33	GND
1	PA00/XIN32/E.0/S1.0/T2.0/C.2	34	VDDIO
2	PA01/XOUT32/E.1/S1.1/T2.1/C.3	35	PA16/E.0/S1+0/S3+0/T2.0/T0.6/G.2
3	PA02/E.2/A.0/A.4/(VOUT)	36	PA17/E.1/S1+1/S3+1/T2.1/T0.7/G.3
4	PA03/E.3/A.1/A.5/VREFA	37	PA18/E.2/S1.2/S3.2/U4.0/T0.2/C.0
5	PB04/E.4/(A.6)	38	PA19/E.3/S1.3/S3.3/U4.1/T0.3/C.1
6	PB05/E.5/A.6/(A.7)	39	PB16/E.0/U2.0/T0.4/G.2/(S5+0)
7	GNDANA	40	PB17/E.1/U2.1/T0.5/G.3/(S5+1)
8	VDDANA	41	PA20/E.4/S3.2/U3.0/T0.6/G.4/(S5.2)
9	PB06/E.6/A.7/(A.8/INN.2)	42	PA21/E.5/S3.3/U3.1/T0.7/G.5/(S5.3)
10	PB07/E.7/(A.9/INP.2)	43	PA22/E.6/S3+0/U0.0/T0.4/G.6/(S5+0)
11	PB08/E.8/A.2/U0.0/(A.4/INN.1/S4.0)	44	PA23/E.7/S3+1/U0.1/T0.5/G.7/(S5+1)
12	PB09/E.9/A.3/U0.1/(A.5/INP.1/S4.1)	45	PA24/E.12/S3.2/U1.0/T1.2/C.2/(S5.2/CAN0.TX)
13	PA04/E.4/A.4/A.0/S0.0/T0.0/(VREFB)	46	PA25/E.13/S3.3/U1.1/T1.3/C.3/(S5.3/CAN0.RX)
14	PA05/E.5/A.5/A.1/S0.1/T0.1	47	GND
15	PA06/E.6/A.6/A.2/S0.2/T1.0/(INN.0)	48	VDDIO
16	PA07/E.7/A.7/A.3/S0.3/T1.1/(INP.0)		

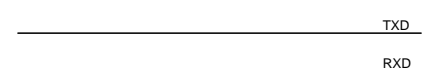
シリアル通信0 (フロー制御無し)



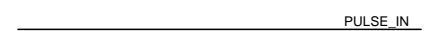
LCD制御



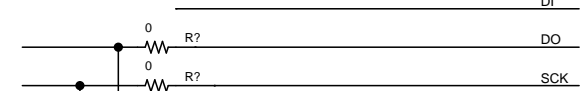
CAN通信1



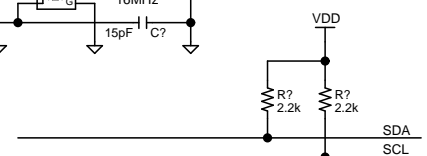
キャプチャ入力 (TCC2)



SPI (シリアル通信2)



I2C (シリアル通信1)



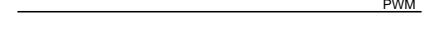
音階出力 (TC4)



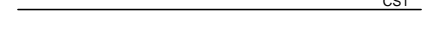
LCD制御



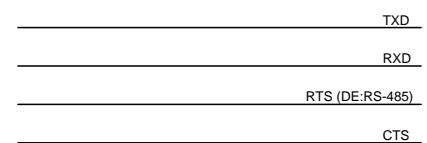
PWM出力 (TC2)



LCD制御



シリアル通信3 (RS485/フロー制御有り)



TITLE		DRAWING_No.	
SAMC20/C21ベース回路 (端子割り当て検討用)			
SHEET	DATE	DESIGN	
1 / 1	2019/02/24	てきーらサンドム	